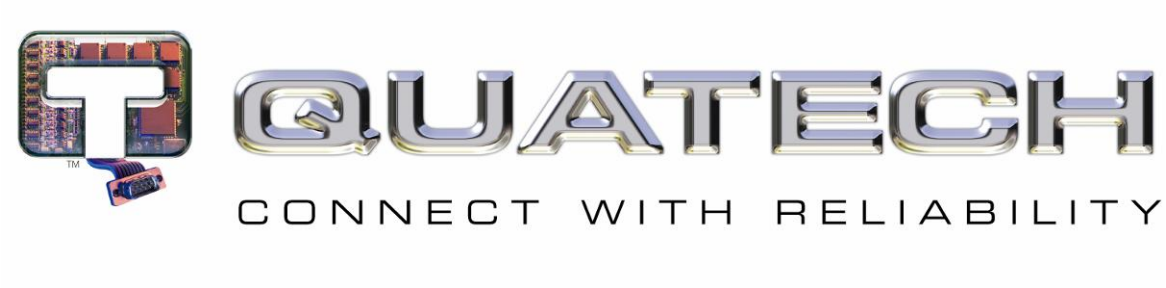

Product Specification

802.11b/g High Performance Enterprise Device Server

Revision: 1.1

August 2009

File name: **databook wlng dp500 family.doc**

Document Number: **100-8080-110**

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Disclaimer

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Contents

Figures

Tables

1.0 Conventions

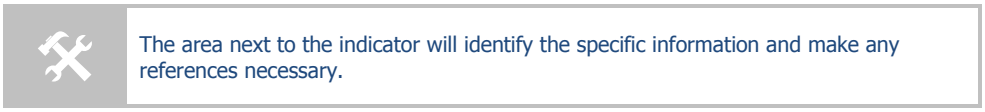
The following section outlines the conventions used within the document, where convention is deviated from the deviation takes precedence and should be followed. If you have any question related to the conventions used or clarification of indicated deviation please contact Quatech Sales or Wireless Support.

1.1 Terminology

Airborne Enterprise Device Server and AirborneDirect Enterprise Device Server is used in the opening section to describe the devices detailed in this document, after this section the term ***module*** will be used to describe the devices.

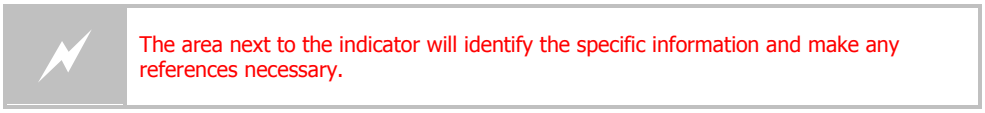
1.2 Notes

A note contains information that requires special attention. The following convention will be used. The area next to the indicator will identify the specific information and make any references necessary.



1.3 Caution

A caution contains information that, if not followed, may cause damage to the product or injury to the user. The shaded area next to the indicator will identify the specific information and make any references necessary.



1.4 File Format

These documents are provided as Portable Document Format (PDF) files. To read them, you need Adobe Acrobat Reader 4.0.5 or higher. For your convenience, Adobe Acrobat Reader is provided on the Radio Evaluation Kit CD. Should you not have the CD, for the latest version of Adobe Acrobat Reader, go to the Adobe Web site (www.adobe.com).

2.0 Product Description

The WLNG-AN-DP500 family is the latest generation of 802.11 wireless device servers from Quatech. The radio features the following:

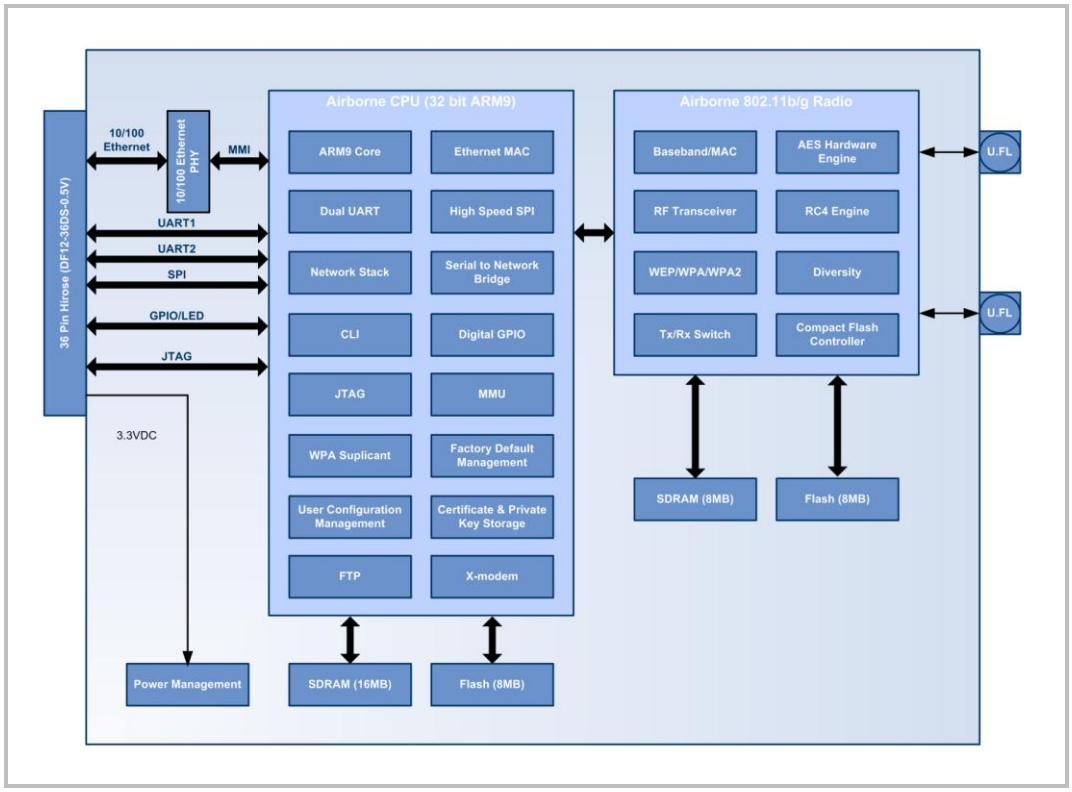
- 802.11b/g WiFi Radio with 32bit ARM9 CPU (128Mb SDRAM, 64Mb Flash)
- Supports WEP, WPA, WPA2 and 802.1x Supplicant, with Certificates.
- The wireless device server includes integrated:
  - 802.11b/g radio driver
  - TCP/IP stack, UDP, telnet, FTP server
  - Data bridging and buffering
  - Command Line Interface
  - Web interface
  - WPA Supplicant
  - 802.11 Radio Driver
- Supports antenna diversity
- Operating Temperature (-40°C to 85°C)
- Storage temp (-50°C to 125°C)
- 36 pin high density SMT connector (*Hirose DF12-36)*
- Dual (2) Hirose U.FL RF connector for RF antenna
- Multiple host interfaces supported:
  - Dual UART (960K BAUD)
  - Serial (RS232/422/485)
  - SPI
  - 10/100 Ethernet PHY
- Advanced Low power modes
- Rugged mounting options.
- No host driver required
- Small form factor module (Dimensions: 29mm x 21mm x 6.0mm)
- Worldwide Regulatory Support

Figure 1- WLNG-AN-DP500 Module Example

3.0 Block Diagram

The following outlines the block diagram of the radio:

Figure 2 - WLNG-SE/SP/AN/ET-DP500 Block Diagram



4.0 Model Numbers

The following table identifies the model numbers associated with the device server family. Please contact Quatech sales for details, quotes and availability.

Table 1 - Model Numbers

Model Number	Description	WiFi	Interface						Security				RoHS
		802.11b/g	UART	RS232	RS485	SPI	Ethernet	GPIO	WEP	WPA	WPA2	EAP	
WLNG-SE-DP501	802.11b/g, UART Interface with RS232/422/485 Driver Control	•	•	•	•			•	•	•	•	•	•
WLNG-SP-DP501	802.11b/g, SPI Interface	•				•		•	•	•	•	•	•
WLNG-AN-DP501	802.11b/g, UART Interface	•	•	•	•			•	•	•	•	•	•
WLNG-ET-DP501	802.11b/g, 10/100 Ethernet Interface	•					•	•	•	•	•	•	•
Eval Kit													
WLNG-EK-DP501	802.11b/g Enterprise Class Serial Device Server Module Eval Kit (inc. WLNG-SE/AN-DP501)												•
WLNG-EK-DP502	802.11b/g Enterprise Class SPI Device Server Module Eval Kit (inc. WLNG-SP-DP501)												•
WLNG-EK-DP503	802.11b/g Enterprise Class Ethernet Bridge Module Eval Kit (inc. WLNG-ET-DP501)												•

5.0 Pin out and Connectors

Pin definition is dependent upon the device type selected. The specific pin function is defined in Table 2 for each device type. Where multiple options are available for a single device type, these options are software selectable by the device firmware.

Table 2 – Module Pin Definition

Pin	Name	Device Type	Description
1	GND	All	Digital Ground
2	TDI	All	JTAG: Test data in
3	VDD	All	3.3VDC
4	VDD	All	3.3VDC
5	RTCK	All	JTAG: Return Test Clock
6	DTXD	All	D_{OUT} Debug
7	/RESET	All	Module RESET
8	DRXD	All	D_{IN} Debug
9	RXD2	UART	D_{IN} UART2
	RXD2	Serial	D_{IN} UART2
	RXD2	SPI	D_{IN} UART2
	RXD2	Ethernet	D_{IN} UART2
	G6	All	GPIO
10	TDO	All	JTAG: Test data out
11	/FRESET	All	Factory RESET
12	CTS1	UART	Clear-to-Send UART1
	CTS	Serial	Clear-to-Send
	/SPI_SEL	SPI	SPI Select
	CTS1	Ethernet	Clear-to-Send UART1
	F5	All	GPIO
13	NC	UART	No Connect
	NC	Serial	No Connect
	NC	SPI	No Connect
	RX+	Ethernet	Ethernet RX+
14	NC	UART	No Connect
	NC	Serial	No Connect
	NC	SPI	No Connect
	RX-	Ethernet	Ethernet RX-
15	GND	All	Digital Ground
16	GND	All	Digital Ground
17	RTS2	UART	Ready-to-Send UART2
	/TXEN	Serial	Line Driver Tx enable
	RTS2	SPI	Ready-to-Send UART2
	RTS2	Ethernet	Ready-to-Send UART2
	G2	All	GPIO
18	RTS1	UART	Ready-to-Send UART1
	RTS	Serial	Ready-to-Send
	SPI_CLK	SPI	SPI Clock Input
	RTS1	Ethernet	Ready-to-Send UART1

Pin	Name	Device Type	Description
	F4	All	GPIO
19	CTS2	UART	Clear-to-Send UART2
	RXEN	Serial	Line driver Rx enable
	CTS2	SPI	Clear-to-Send UART2
	CTS2	Ethernet	Clear-to-Send UART2
	G1	All	GPIO
20	TCK	All	JTAG: Test clock
21	TXD2	UART	D_{OUT} UART2
	TXD2	Serial	D_{OUT} UART2
	TXD2	SPI	D_{OUT} UART2
	TXD2	Ethernet	D_{OUT} UART2
	G7	All	GPIO
22	G0	UART	GPIO
	SER_MODE	Serial	Serial interface type selection (RS232/422/485)
	SPI_INT	SPI	SPI Interrupt
	G0	Ethernet	GPIO
23	LED_CON	All	Valid TCP/IP Connection Indicator
	F6		GPIO
24	RXD1	UART	D_{IN} UART1
	RXD1	Serial	D_{IN} UART1
	MOSI	SPI	D_{IN} SPI
	RXD1	Ethernet	D_{IN} UART1
	F7	All	GPIO
25	LED_POST	All	POST Status Indicator
	F0		GPIO
26	LED_WLN_CFG	All	Module TCP/IP Configuration Indicator
	F3		GPIO
27	LED_RF_LINK	All	Module RF Link Status Indicator
	F2		GPIO
28	TXD1	UART	D_{OUT} UART1
	TXD	Serial	D_{OUT}
	MISO	SPI	D_{OUT} SPI
	TXD1	Ethernet	D_{OUT} UART1
	F1	All	GPIO
29	NC	UART	No Connect
	NC	Serial	No Connect
	NC	SPI	No Connect
	TX-	Ethernet	Ethernet TX-
30	NC	UART	No Connect
	NC	Serial	No Connect
	NC	SPI	No Connect
	TX+	Ethernet	Ethernet TX+
31	NTRST	All	JTAG: Test RESET signal
32	TMS	All	JTAG: Test mode select
33	VDD	All	3.3VDC
34	VDD	All	3.3VDC
35	LED_RF_ACT	All	Radio Status Indicator, driven by the radio.
36	GND	All	Digital Ground

5.1 Digital UART Ports

The units supports two digital UART ports, use of these ports is determined by the device type choice made in firmware. The details of the ports can be seen in Table 3.

The availability of UART2 for these device types is selected in firmware.

Table 3 - UART Pin Definition

Device Type	UART		Serial		All
Pin Definition	UART1 Pin	UART2 Pin	UART1 Pin	UART2 Pin	Debug
Data out (D_{OUT})	28	21	28	21	6
Data In (D_{IN})	24	9	24	9	8
Clear-to-Send (CTS)	12	19	12		
Ready-to-Send (RTS)	18	17	18		
Transmit Enable (/TXEN)			17		
Receive Enable (/RXEN)			19		
Serial Mode (SER_MOD)			22		

The primary UART supports a 4-wire interface; the secondary port supports 4-wire interface except when being used with the Serial Device type, in which case it is reduced to a 2-wire only.

The primary digital UART can be used as the primary connection for the Serial device type. This type supports a 7-wire interface to allow the definition of the serial interface type (RS232/3422/485) and the data transfer direction. Definitions of this interface can be seen in Table 3.

The UART1 and UART2 interfaces support the following configurations:

- BAUD: 300, 600, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800, 921600
- Flow Control: None, Hardware (CTS/RTS), Software (XON/XOFF)
- Default settings: 9600, 8, N, 1, No Flow Control.

5.2 Ethernet PHY Port

A 10/100 Ethernet PHY interface is supported when the Ethernet device type is selected in firmware. This interface is a 10/100Mbps interface that supports auto negotiation and cross-over cabling. The interface also supports both half and full duplex for 10Mbps and 100Mbps.

The interface uses a Broadcom BCM5241A Ethernet PHY, please refer to the manufacturers datasheet for interface details and appropriate design guidelines.

5.3 Serial Peripheral Interface (SPI)

Please refer to section 7.0 for details on this interface.

5.4 Debug/Console Port

A debug/console port is supported by a 2-wire serial interface defined in Table 3. This port is a bidirectional serial port intended for debug of the unit only, it does not support data transfer.

It is recommended that a connection to this port be supported via test points or a two pin header. The default settings for the debug port are 115200, 8, N 1, No Flow Control.

CAUTION: Do not use the debug port without contacting Quatech Technical Support first. Potential damage to the module may occur.

5.5 General Purpose Input/Output (GPIO)

A number of the interface pins support multiple functional definitions. Those defined as alternately GPIO pins can be selected as such via device firmware.

The GPIO pins are digital I/O capable of supporting up to a 16mA drive current at 3.3VDC.

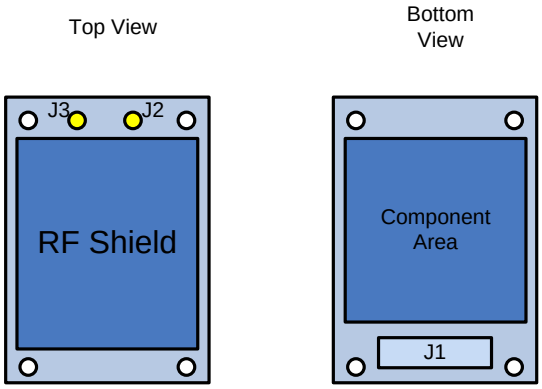
5.6 Connector Definition

There are a total of three connectors to the radio:

J1: 36 pin Digital Host interface.
Hirose: ***DF12-36DP-0.5V(XX)*** *(0.50mm (.020") Pitch Plug, Surface Mount, Dual Row, Vertical, 4.00mm Stack Height, 36 Circuits)*

J2: Primary RF connector for 802.11b/g antenna.
Hirose U.FL

J3: Secondary RF connector for 802.11b/g antenna.
Hirose U.FL.



6.0 Electrical & RF Specification

Table 4- Absolute Maximum Values[1]

Parameter	Min	Max	Unit
Maximum Supply Voltage	-0.3	4.0	VDC
Power Dissipation		2.00	W
Operating Temperature Range	-40	85	°C
Storage Temperature	-50	125	°C

Note: 1. Values are absolute ratings, exceeding these values may cause permanent damage to the device.

Table 5 – Operating Conditions & DC Specification

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply Voltage	3.00	3.30	3.60	V
V_{IL}	Input Low Level Voltage	-0.3		0.8	
V_{IH}	Input High Level Voltage	2.0		V_{DD} + 0.3	
V_{OL}	Output Low Level Voltage			0.4	
V_{OH}	Output High Level Voltage	V_{DD} - 0.4			
I_{CCTXG}	Operating Current – UART Data In (802.11g) *Transmitting @ 54Mb/s* *UART 100% Duty Cycle @ 920K BAUD*		340	360	mA
I_{CCRXG}	Operating Current – UART Data Out (802.11g) *Receiving valid packets @ 54Mb/s* *UART 100% Duty Cycle@ 920K BAUD*		480	490	mA
I_{CCTXB}	Operating Current – UART Data In (802.11b) *Transmitting @ 11Mb/s* *UART 100% Duty Cycle @ 920K BAUD*		340	360	mA
I_{CCRXB}	Operating Current – UART Data Out (802.11b) *Receiving valid packets @ 11MB/s* *UART 100% Duty Cycle @ 920K BAUD*		480	490	mA
I_{CCTXG_ETH}	Operating Current – Ethernet Data In (802.11g) *Transmitting @ 54Mb/s* *10/100 Ethernet 100% Duty Cycle*		470	500	mA
I_{CCRXG_ETH}	Operating Current – Ethernet Data Out (802.11g) *Receiving @ 54Mb/s* *10/100 Ethernet 100% Duty Cycle*		520	560	mA

Symbol	Parameter	Min	Typ	Max	Units
I_{CCTXB_ETH}	Operating Current – Ethernet Data In (802.11b) *Transmitting @ 11Mb/s* *10/100 100% Duty Cycle*		520	560	mA
I_{CCRXB_ETH}	Operating Current – Ethernet Data Out (802.11b) *Receiving @ 11Mb/s* *10/100 Ethernet 100% Duty Cycle*		500	530	mA
I_{CCU}	Radio and CPU on. No data traffic (UART)		340	360	mA
I_{CCE}	Radio and CPU on. No data traffic (Ethernet)		330	350	mA
I_{SBU0}	Radio off (UART) *CPU Idle, radio off (f/w control)*		350	360	mA
I_{SBE0}	Radio off (Ethernet) *CPU Idle, radio off (f/w control)*		360	370	mA
I_{SB1}	Doze Mode *IEEE PSPoll mode, Associated, Idle, Beacon Interval = 100ms* *CPU Idle, wake on UART or Network traffic*	140		210	mA
I_{SB3U}	Sleep Mode – UART/Serial *Radio in Deep Sleep (disassociated)* *CPU Idle, wake on UART traffic*		102		mA
I_{SB3E}	Sleep Mode – Ethernet *Radio in Deep Sleep (disassociated)* *CPU Idle, wake on pm-mode*		95		mA

Table 6 - RF Characteristics – 802.11b/g

Symbol	Parameter	Rate (Mb/s)	Min	Average dBm / mW		Peak dBm / mW		Units
P_{OUTB}	Transmit Power Output 802.11b	11, 5.5, 2, 1		15.0	31.6	20.0	100	dBm
P_{OUTG}	Transmit Power Output 802.11g	48, 54		12.7	18.6	17.7	58.9	dBm
		24, 36		15.0	31.6	20.0	100	
		12, 18		15.9	38.9	20.9	123	
		6, 9		16.0	39.8	21.0	125.9	
P_{RSENB}	Receive Sensitivity 802.11b	11		-82				dBm
		1		-91				
P_{RSENG}	Receive Sensitivity 802.11g	54		-68				dBm
		36		-78				
		18		-80				
		6		-86				
$F_{RANGEBG}$	Frequency Range		2412			2484		MHz

Table 7 - Supported Data Rates by Band

Band	Supported Data Rates (Mb/s)
802.11b	11, 5.5, 2, 1
802.11g	54, 48, 36, 24, 18, 12, 9, 6

Table 8 - Operating Channels

Band	Region	Freq Range (GHz)	No. of Channels	Channels
802.11b	US/Canada	2.401 - 2.473	11	1 – 11
	Europe	2.401 - 2.483	13	1 – 13
	France	2.401 - 2.483	4	10 – 13
	Japan	2.401 - 2.495	14	1 – 14
802.11g	US/Canada	2.401 - 2.473	11	1 – 11
	Europe	2.401 - 2.483	13	1 – 13
	France	2.446 - 2.483	4	10 – 13
	Japan	2.401 - 2.483	13	1 – 13

1. Only channels 1, 6 and 11 are non-overlapping.

Table 9 - RF Characteristics – 802.11b/g

Symbol	Parameter	Rate (Mb/s)	Min dBm	Average dBm / mW		Peak dBm / mW		Units
P_{OUTB}	Transmit Power Output 802.11b	11, 5.5, 2, 1	13	15	31.6	19.3	85.1	dBm/mW
P_{OUTG}	Transmit Power Output 802.11g	6, 9,12,18, 24, 36, 48, 54	10	12	15.9	21.5	141.3	dBm/mW
P_{RSENB}	Receive Sensitivity 802.11b	11		-84				dBm
		5.5		-85				
		2		-86				
		1		-86				
P_{RSENG}	Receive Sensitivity 802.11g	54		-69				dBm
		48		-70				
		36		-74				
		24		-78				
		18		-81				
		12		-83				
		9		-85				
		6		-86				
$F_{RANGEBG}$	Frequency Range		2412			2484		MHz

6.1 AC Electrical Characteristics – Transmitter

Transmit power is automatically managed by the device for minimum power consumption. The MAXIMUM transmit power at the RF connector is typically +15dBm ± 2 dB for B-Mode (all rates) and +12dBm+/-2dB for G-Mode (all rates).

6.2 Performance/Range

The following table illustrates the typical data rates, performance and range the device is capable of providing using an omni directional antenna.

Table 10 - Radio Typical Performance Range

Data Rate	Typical Outdoor Distance (Unity gain antenna)	Typical Outdoor Distance (2dBi antenna gain on each end for B/G mode)
1.0 Mb/s	240m	380m
11.0 Mb/s	135m	215m
6Mb/s 802.11g	135m	215m
6Mb/s 802.11a	49m	155m
54Mb/s 802.11g	12m	19m
54Mb/s 802.11a	4.5m	14m

Ranges are based on receiver sensitivity, Transmitter power, free-space path loss estimates, antenna gain factors, and link margin estimates. Actual range will vary from those stated. Non-line-of-site applications will result in typical values less than shown above.

The Data Rate is the supported connection rate for the wireless link, the actual data throughput for the link will be less than the stated data rates.

7.0 SPI Interface

The following section details the SPI interface specification for both hardware timing and SPI protocol. The device is a SPI slave and requires a compatible SPI master for operation.

7.1 Pinout

When the SPI interface is enabled, through the CLI or web interface, the following pins are assigned for communication.

Table 11 - SPI Pinout Details

Pin Definition	SPI	UART2 Pin	Debug
Master In Slave Out (MISO)	28		
Master Out Slave In (MOSI)	24		
SPI Interrupt (SPI_INT)	22		
SPI Clock (SPI_CLK)	18		
SPI Select (/SPI_SEL)	12		
Data In (RxD2, DTXD)		9	8
Data out (TxD2, DRXD)		21	6
Ready-to-Send (RTS2)		17	
Clear-to-Send (CTS2)		19	

Table 12 - SPI Signal Descriptions

Pin Definition	Description
Master In Slave Out (MISO)	Serial Data OUT; must be connected to the serial data in of the master.
Master Out Slave In (MOSI)	Serial Data IN; Must be connected to the serial data out of the master.
SPI Interrupt (SPI_INT)	Interrupt signal driver by slave see Table 16 for details of operation.
SPI Clock (SPI_CLK)	SPI clock sourced from the master.
SPI Select (/SPI_SEL)	Enable the SPI slave, sourced from the master. Active low signal.

7.2 SPI AC Characteristics

The following specification identifies the required hardware timing to successfully implement a SPI interface with the Airborne Device Server module.

Table 13 - SPI AC Timings

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX}	Maximum Clock Frequency			8.00	MHz
t_{CS}	SPI Select Low to Clock Rising Edge	100			ns
t_{CH}	Clock High	62.5			ns
t_{CL}	Clock Low	62.5			ns
t_{DA}	Clock High to Data Out			60	ns
t_{DS}	Clock Low to Data In Valid Set-up time	14			ns
t_{DH}	Clock Low to Data Valid Hold time	2			ns
t_{CSH}	Clock Falling Edge to SPI Select High	100			ns
t_{DELAY}	SPI Select High to SPI Select Low	40			ns

Figure 3 - SPI Read/Write Timing

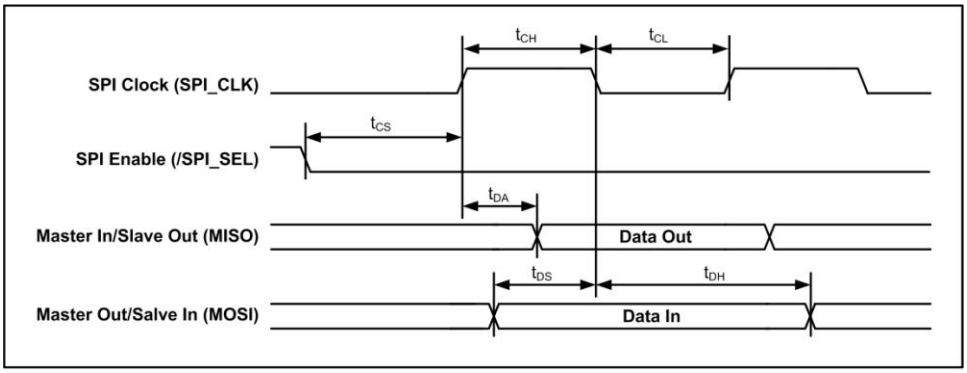
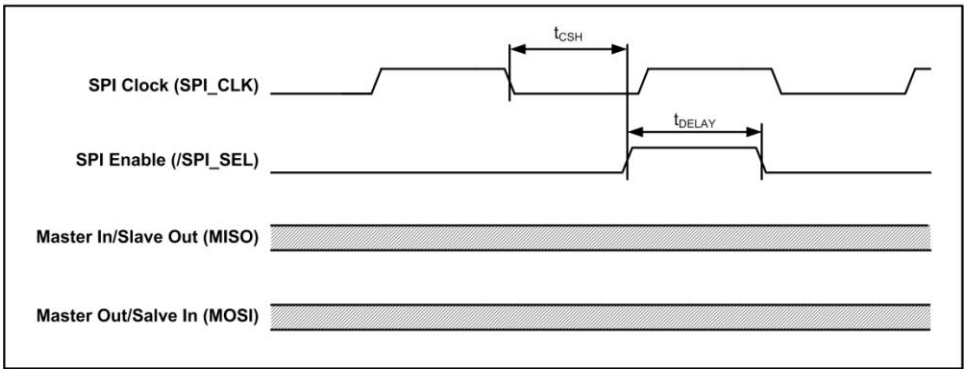


Figure 4 - SPI Clock and Select Timing



7.3 SPI Protocol

A SPI message is composed of a 4 byte header followed by 0 or more bytes of data. The header data is full-duplex. That is, the Tx message header is sent to

the Airborne Device Server module by the host at the same time the Rx message header is sent to the host from the Airborne Device Server.

The Tx message header consists of a Command (CMD) byte, followed by three Parameter (PARM) bytes. They are described in the SPI Commands section (7.4) below.

The Rx message header consists of a Rx Data Available field, and a Tx Buffer Available field. The Rx Data Available field indicates the number of data bytes the Device Server has available for the host. They can be received by the RXDATA command. The Tx Buffer Available field indicates how many data bytes the Device Server is able to accept from the host. This data is to be shifted in by the host using the TXDATA (Table 16) command. Both fields are 16 bit values and are stored in little-endian format (LSB first).

Table 14 - Tx Message Header

0	1	2	3
CMD	PARAM1	PARAM2	

Table 15 - Rx Message Header

0	1	2	3
Rx Data Available		Tx Buffer Available	

7.4 SPI Commands

The following commands are available for use in the CMD message header.

Table 16 - SPI Command Description

Command (Hex)	Name	Description
0x00	NOP	The NOP command does nothing. It is intended to be used when the host wants to simply retrieve the Rx Message Header without any other operation.
0x04	BREAK	The BREAK command will issue a break sequence to the module. It is analogous to the BREAK signal on a common UART.
0x08	TXINTCLR	The TXINTCLR command will clear the Tx interrupt. Use this command when the module is issuing a Tx interrupt but there is no more data to send. This is analogous to the reset Tx interrupt command on a common UART.

Command (Hex)	Name	Description
0x10	INTENA	The INTENA command will enable interrupts from the module. For this command, the PARM1 field will define the interrupts to be enabled. The definition of the PARM1 field is as follows: **B7** **Interrupt Sense** – Determines the asserted state of the interrupt pin. If this bit is set, the interrupt pin will be active high, otherwise the interrupt pin will be active low. **B1** **TX Interrupt** – If this bit is set, the interrupt pin will be asserted when there is space available in the Tx buffer. **B0** **RX Interrupt** – If this bit is set, the interrupt pin will be asserted when there is Rx data available.
0x20	INTDIS	The INTDIS command will disable interrupts from the module. For this command, the PARM1 field will define the interrupts to be disabled. The definition of the PARM1 field is as follows: **B1** **TX Interrupt** – If this bit is set, The Tx interrupt function will be disabled. **B0** **RX Interrupt** – If this bit is set, the Rx interrupt function will be disabled.
0x40	TXDATA	The TXDATA command is used to send data to the module to be transmitted on the wireless link. The host may send at most the number of bytes indicated by the Tx Buffer Available field in the Rx Message Header. The actual length sent by the host is determined by the 16 bit value in PARM2. The value in PARM2 is little-endian (LSB first) and must be less than or equal to the number in the Tx Buffer Available field. Any bytes sent in excess of this number will be ignored.
0x80	RXDATA	The RXDATA command is used to receive data from the module that has been received on the wireless link. The host may receive at most the number of bytes indicated by the Rx Data Available field in the Rx Message Header. The actual number of bytes received by the host is determined by the 16 bit value in PARM2. The value in PARM2 is little-endian (LSB first) and must be less than or equal to the number in the Rx Data Available field. If additional clock cycles are sent to the module beyond this number, meaningless data will be returned.

The TXDATA and RXDATA commands can be combined for full-duplex operation. For example, a command byte of **0xC0** would be a TXDATA and RXDATA command combined. The result of this command would be that the module would accept data being shifted in as Tx data, while at the same time, Rx data would be shifted out. In this case, the number of bytes transferred for TXDATA must be equal to the number of bytes transferred for RXDATA. The PARM2 parameter will indicate the number of bytes to be transferred for both the TXDATA and RXDATA commands.

8.0 Antenna

The unit supports antenna connection through a single Hirose U.FL connector, located on the top surface of the radio next to the RF shielding.

Any antenna used with the system must be designed for operation within the 2.4GHz ISM band and specifically must support the 2.412GHz to 2.482GHz for 802.11b/g operation. They are required to have a VSWR of 2:1 maximum referenced to a 50ς system impedance.

8.1 Antenna Selection

The Airborne radio supports a number of antenna options, all of which require connection to the U.FL connectors on the radio. Ultimately the antenna option selected will be determined by a number of factors, these include consideration of the application, mechanical construction and desired performance. Since the number of possible combinations is endless we will review some of the more common solutions in this section. If your application is not covered during this discussion please contact Technical Support for more specific answers.

The available antenna connections include:

- Host board mounted antenna
- Host Chassis mounted antenna
- Embedded antenna

In addition to the above options, location and performance need to be considered, the following sections discuss these items.

8.2 Host Board Mounted Antenna

Host board mounted requires that an antenna connection is physically mounted to the host system board. It also requires that the host board include a U.FL connector (two (2) if diversity is being used) to allow a U.FL to U.FL coaxial lead to connect from the radio to the host board. It will then require 50ς matched PCB traces to be routed from the U.FL connector to the antenna mount.

There are several sources for the U.FL to U.FL coaxial cable these include Hirose, Sunridge and IPEX. Please contact Quatech for further part numbers and supply assistance.

This approach can simplify assembly but does require that the host system configuration can accommodate an antenna location that is determined by the host PCB. There are also limitations on the ability to seal the enclosure when using this approach.

This approach also restricts the selection of available antenna. When using this approach, antennas that screw or press fit to the PCB mount connector must be used. There are many options for the antenna connector type, however if you wish to utilize the FCC/IOC modular approval the connector choice must comply

with FCC regulations, these state a non-standard connector is required e.g. TNC/SMA are not allowed, RP-TNC/RP-SMA are allowed.

8.3 Host Chassis Mounted Antenna

Host Chassis mounted antennas require no work on the host PCB. They utilize an antenna type called 'flying lead'. There are two types of flying leads; one which provides a bulkhead mounted antenna connector and one which provides a bulk head mounted antenna. The type you choose will be determined by the application.

A flying lead system connects a U.FL coaxial lead to the radio's U.FL connector, the other end of the coax is attached to either a bulkhead mounted antenna connector or directly to an antenna that has an integrated bulkhead mount.

In either of the two cases, the use of this approach significantly reduces the antenna system development effort and provides for greater flexibility in the available antenna types and placement in the host system chassis.

When using the flying lead antenna (integrated bulk head mounting), there are no connector choice restrictions for use with the FCC/IOC modular certification. However if the flying lead connector is used, the same restrictions as identified for the Host Mounted Antenna apply.

There are many suppliers of flying lead antenna and connectors; Quatech's Airborne Antenna product line offers a range of antenna solutions.

8.4 Embedded Antenna

Use of Embedded antenna can be the most interesting approach for M2M, industrial and medical applications. Their small form factor and absence of any external mounting provides a very compelling argument for their use. There is a downside to this antenna type and it comes with performance. Antenna performance for all of the embedded options will, in most cases, be less that that achievable with external antenna. This does not make them unusable; it will impact choice of antenna type and requires more focus on placement.

The three main embedded antenna types are PCB embedded, chip (PCB mounted) and flying lead; each has its advantages and disadvantages (See Table 17).

Table 17 - Embedded Antenna Options

Antenna Type	Features			
	Cost	Size	Availability	Performance
PCB Embedded	Lowest	Largest	Custom	Poor
Chip	Low	Small	Standard	Poor
Flying Lead	Low	Small	Standard	Fair

PCB Embedded – This approach embeds an antenna design into the host PCB. This approach is very common with add-in WiFi card (CF, PCMCIA, SDIO, etc.) as it requires no external connections and is the cheapest production approach. The lower production cost requires significant development cost and lack of performance and flexibility.

Chip – The integration of a chip antenna is simple and requires a relatively small footprint on the host system, however, it does suffer from the same limitations of flexibility and performance seen with the PCB embedded approach. There are relatively large numbers of suppliers of this type of antenna; there is also a range of configuration and performance options.

Flying Lead – This approach is similar to the flying lead solution for external antennas, the difference is that the form factors are smaller and provide a range of chassis and board mounting options, all for internal use. This approach suffers less from the performance and flexibility limitations of the other approaches, since the location of the antenna it not determined by the host PCB design. The assembly of a system using this approach maybe slightly more complex since the antenna is not necessarily mounted on the host PCBA.

8.5 Antenna Location

The importance of this design choice cannot be over stressed; it can in fact be the determining factor between success and failure of the WiFi implementation.

There are several factors that need to be considered when determining location:

- Distance of Antenna from radio
- Location of host system
  - Proximity to RF blocking or absorbing materials
  - Proximity to potential noise or interference
  - Position relative to infrastructure (Access Points or Laptops)
- Orientation of host system relative to infrastructure
  - Is it known
  - Is it static

To minimize the impact of the factors above the following things need to be considered during the development process:

- Minimize the distance between the radio and the location of the antenna. The coaxial cable between the two impacts the Transmit Power and Receive Sensitivity negatively. Quatech recommends using 1.32-1.37mm outer diameter U.FL coaxial cables.
- Minimize the locations where metal surfaces come into contact or are close to the location of the antenna.
- Avoid locations where RF noise, close to or over lapping the ISM bands, may occur. This would include microwave ovens and wireless telephone systems in the 2.4GHz and 5.0GHz frequency range.
- Mount the antenna as high on the equipment as possible.

- Locate the antenna where there is a minimum of obstruction between the antenna and the location of the Access Points. Typically Access Points are located in the ceiling or high on walls.
- Keep the main antenna's polarization vertical, or in-line with the antenna of the Access Points. 802.11 systems utilize vertical polarization and aligning both transmit and receive antenna maximizes the link quality.

Even addressing all of the above factors, does not guarantee a perfect connection, however with experimentation an understanding of the best combination will allow a preferred combination to be identified.

8.6 Performance

Performance is difficult to define as the appropriate metric changes with each application or may indeed be a combination of parameters and application requirements. The underlying characteristic that, in most cases, needs to be observed is the link quality. This can be defined as the bandwidth available over which communication, between the two devices, can be performed, the lower the link quality the less likely the devices can communicate.

Measurement of link quality can be made in several ways; Bit Error Rate (BER), Signal to Noise (SNR) ratio, Signal Strength and may also include the addition of distortion. The link quality is used by the radio to determine the link rate, generally as the link quality for a given link rate drops below a predefined limit, the radio will drop to the next lowest link rate and try to communicate using it.

The reciprocal is also true, if the radio observes good link quality at one rate it will try to move up to the next rate to see if communication can be sustained using it. It is important to note that for a given position the link quality improves as the link rate is reduced. This is because as the link rate drops the radios Transmit power and Receive sensitivity improve.

From this it can be seen that looking at the link rate is an indirect way of assessing the quality of the link between the device and an Access Point. You should strive to make the communication quality as good as possible in order to support the best link rate. However be careful not to *over specify* the link rate. Consider your applications bandwidth requirements and tailor your link rate to optimize the link quality e.g. the link quality for a location at 6Mb/s is better than it would be for 54Mb/s, if the application only needs 2Mb/s of data throughput, the 6Mb/s rate would provide a better link quality.

Aside from the radio performance, there are a number of other things that contribute to the link quality; these include the items discussed earlier and choices made when looking at the overall antenna gain. The antenna gain contributes to the Equivalent Isotropically Radiated Power (EIRP) of the system. This is part of an overall measurement of the link quality called link margin.

Link Margin provides a measure of all the parts of the RF path that impact the ability of two systems to communicate. The basic equation looks like this:

EIRP (dB) = TxP + TxA – TxC

Link Margin (dB) = EIRP – FPL + (RxS + RxA – RxC)

Where:
TxP = Transmitter output power (dBm)
TxA = Transmitter antenna gain (dBi)
TxC = Transmitter to Antenna coax cable loss (dB)
FPL = Free Path Loss (dB)
RxS = Receiver receive sensitivity (dBm)
RxA = Receiver antenna gain (dBi)
RxC = Receiver to Antenna coax cable loss (dB)

This is a complex subject and requires more information than is presented here, Quatech recommends at reviewing the subject and evaluating any system at a basic level.

It is then possible, with a combination of the above items and an understanding of the application demands, to achieve a link quality optimized for the application and host design. It is important to note that this is established with a combination of hardware selection, design choices and configuration of the radio.

9.0 RESET Function

For correct operation of the on-board Power-on RESET (POR) and internal RESET controllers, the RESET pin on the WLNG-XX-DP500 family must obey the following timing and signal conditions.

Figure 5 - Power on RESET Timing

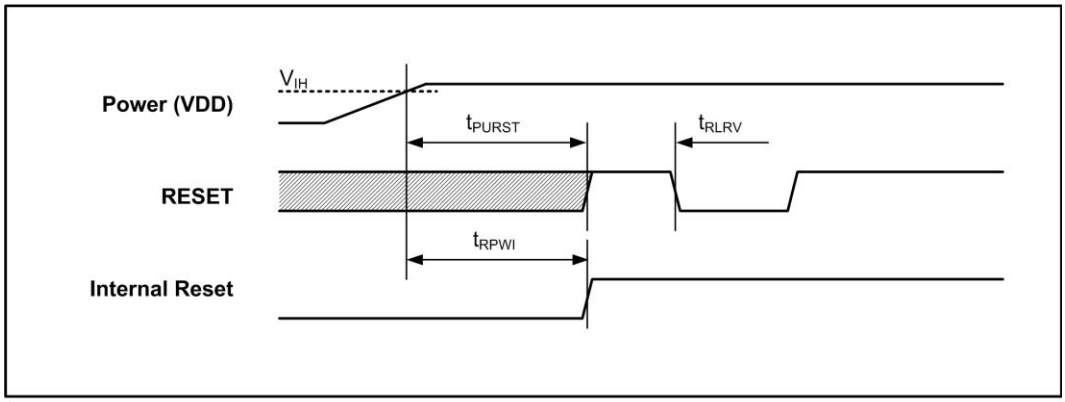


Figure 6 - RESET Timing

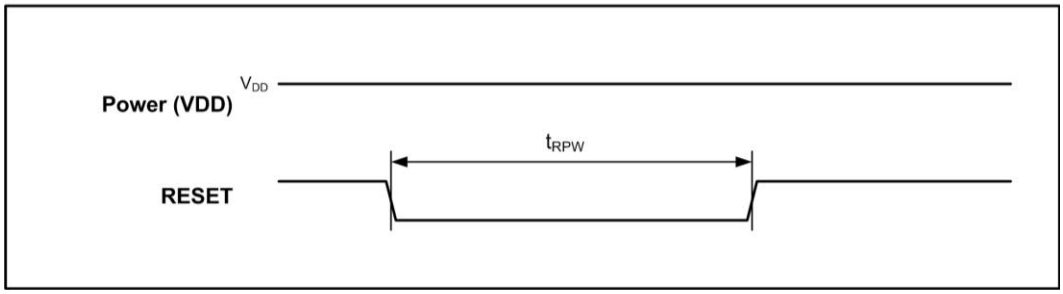
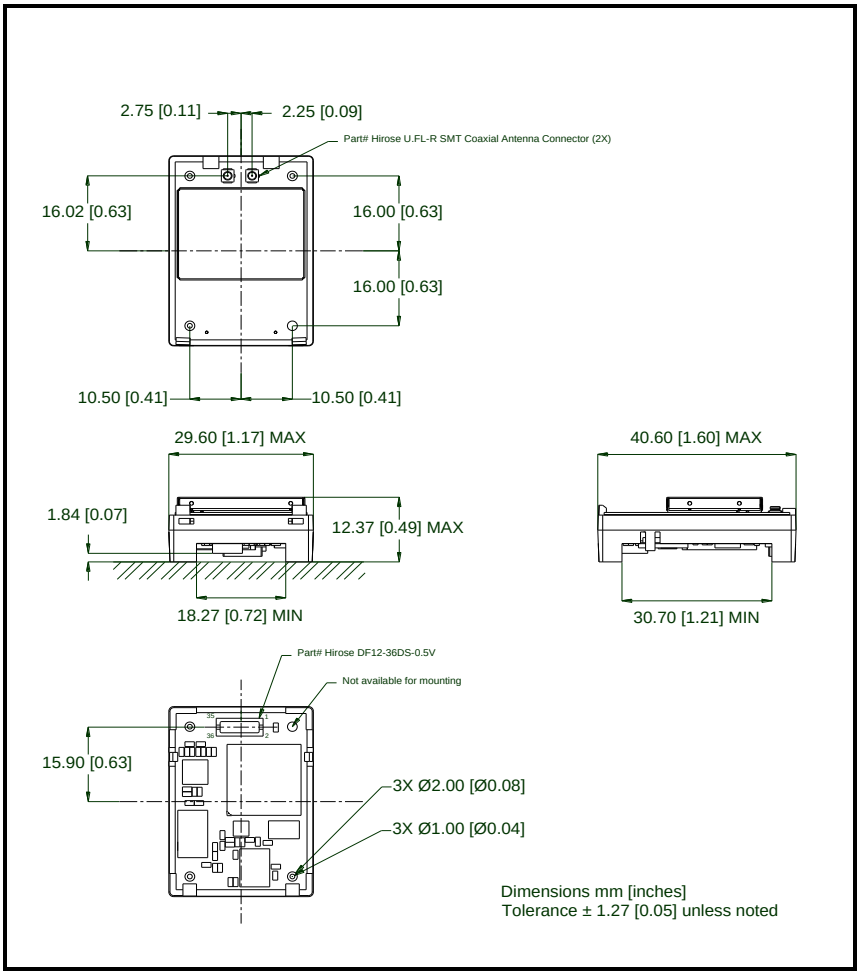


Table 18 - RESET Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{PURST}	Valid V_{DD} to RESET valid			200	ms
t_{RLRV}	RESET Valid to RESET Low	0			ms
t_{RPWI}	Valid V_{DD} to Internal RESET completed			200	ms
t_{RPW}	RESET Pulse Width	100			µs

For Hardware revisions Rev C2 and earlier additional timing constraints apply. Please contact Quatech Technical Support for details.

10.0 Mechanical Outline



Radio Connector: **DF12-36DS-0.5V(XX)** (Hirose)

Hirose: *0.50mm (.020") Pitch Plug, Surface Mount, Dual Row, Vertical, 4.00mm Stack Height, 36 Circuits*

Board Connector: **DF12-36DP-0.5V(XX)** (Hirose)

Hirose: *0.50mm (.020") Pitch Plug, Surface Mount, Dual Row, Vertical, 4.00mm Stack Height, 36 Circuits*

RF Connector: **U.FL**

Hirose: *Ultra Small Surface Mount Coaxial Connector*

Mounting Screw: **3/8 inch length, 0-42 thread Zinc Plated Steel Tri-P Torx Thread-Form Screw for plastic**

McMaster-Carr: *99512A117 (Zinc Plated Steel)*
McMaster-Carr: *96001A107 (Stainless Steel)*

11.0 Certification & Regulatory Approvals

The unit complies with the following agency approvals:

Table 19 - Regulatory Approvals

Country	Standard	Status
North America (US & Canada)	FCC Part 15 Sec. 15.107, 15.109, 15.207, 15.209, 15.247 Modular Approval	Granted
Europe	CISPR 16-1 :1993 ETSI EN 300 328 Part 1 V1.2.2 (2000-07) ETSI EN 300 328 Part 2 V1.1.1 (2000-07)	Completed
Japan	ARIB STD-T71 v1.0, 14 (Dec 2000) ARIB RCR STD-T33 (June 19, 1997) ARIB STD-T66 v2.0 (March 28, 2002)	Pending

11.1 FCC Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

11.2 FCC RF Exposure Statement

To satisfy RF exposure requirements, this device and its antenna must operate with a separation distance of a least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

11.3 Information for Canadian Users (IC Notice)

This device has been designed to operate with an antenna having a maximum gain of 5dBi for 802.11b/g band. An antenna having a higher gain is strictly

prohibited per regulations of Industry Canada. The required antenna impedance is 50 ohms.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (EIRP) is not more than required for successful communication.

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

11.4 FCC/IOC Modular Approval

This document describes the Airborne WLN FCC modular approval and the guidelines for use as outlined in FCC Public Notice (DA-00-1407A1).

The WLRG-RA-DP101 is covered by the following modular grants:

Country	Standard	Grant
North America (US)	FCC Part 15 Sec. 15.107, 15.109, 15.207, 15.209, 15.247 Modular Approval	F4AWLNG1
Canada	RSS 210 Modular Approval	39139A-WLNG1

By providing FCC modular approval on the Airborne WLN modules, the customers are relieved of any need to perform FCC part15 subpart C Intentional Radiator testing and certification, except where they wish to use an antenna that is not already certified.

Quatech supports a group of pre-approved antenna; use of one of these antennas eliminates the need to do any further subpart C testing or certification. If an antenna is not on the list, it is a simple process to add it to the pre-approved list without having to complete a full set of emissions testing. Please contact Quatech Technical support for details of our qualification processes.

Please note that as part of the FCC requirements for the use of the modular approval, the installation of any antenna must require a professional installer. This is to prevent any non-authorized antenna being used with the radio. There are ways to support this requirement but the most popular is to utilize a non-standard antenna connector, this designation includes the reverse polarity versions of the most popular RF antenna types (SMA, TNC, etc.). For more details please contact Quatech.

The following documents are associated with this applications note:

- FCC Part 15 – Radio Frequency Devices
- FCC Public Notice – DA-00-1407A1 (June 26th, 2000)

Quatech recommends that during the integration of the radio, into the customers system, that any design guidelines be followed. Please contact Quatech Technical Support if you have any concerns regarding the hardware integration.

Contact Quatech Technical support for a copy of the FCC and IOC grant certificates, the test reports and updated approved antenna list.

11.5 Regulatory Test Mode Support

The Airborne Device Server includes support for all FCC, IC and ETSI test modes required to perform regulatory compliance testing on the module, please contact Quatech Technical Support for details on enabling and using these modes.

12.0 Physical & Environmental Approvals

The device has passed the following primary physical and environmental tests. The test methods referenced are defined in SAE J1455 Aug1994.

Table 20 - Mechanical Approvals

Test	Reference	Conditions
Temperature Range (Operational)	Table 1B, Type 2b	-40°C to +85°C
Temperature Range (Non-Operational)		-50°C to +125°C
Humidity	Sect 4.2.3	0-95%RH @ 38°C condensing Fig 4a – 8 hours active humidity cycle
Altitude	Sect 4.8	Operational: 0-12,000ft (62 KPa absolute pressure) Non-operational: 0-40,000ft (18.6 KPa absolute pressure)
Vibration	Sect 4.9	Operational: 2.4 Grms, 10-1K Hz, 1hr per axis Non-operational: 5.2 Grms, 10-1K Hz, 1hr per axis
Shock	Sect 4.10	Operational: 20Gs MAX, 11ms half-sine pulse
Product Drop	Sect 4.10.3.1	1m onto concrete, any face or corner, 1 drop
Packaging Drop	Sect 4.10.2.1	32 inches onto concrete on each face and corner. Packaged in 'for transit' configuration.
Accelerated Life Test	MIL-STD-883 Method 1015	1000hrs @ 125°C, static bias

Test reports are available from Quatech Technical Support, please contact directly for the latest documentation.

13.0 Change Log

The following table indicates all changes made to this document:

Version	Date	Section	Change Description	Author
1.0	04/16/2009	-	Initial Release	ACR
1.1	08/11/2009	3.0	Updated block diagram with SPI interface.	ACR
		5.0	Table 2: Removed reference to GPIO on pin 35	
		5.3	Added section 5.3 SPI interface section.	
		6.0	Table 4.0: Changed maximum voltage to 4.0VDC	
			Table 5.0: Updated Power state labels and values	
		7.0	Added section 7.0 SPI interface specification.	
		11.5	Added reference to Regulatory Test Mode Support in module	
		12.0	Table 16: Removed reference to Salt Spray environmental test.	